• Features

- Provides the logic to request and gain control of the UNIBUS
- Used to arbitrate for DMA or interrupt mastership
- Bus receivers and drivers compatible with UNIBUS
- Used to develop UNIBUS interfaces for peripheral devices

• Description

The DC013 is a 16-pin, dual-inline package (DIP) used in the development of device interfaces for the UNIBUS. It contains the logic required to perform interrupt bus requests (BR) and nonprocessor direct memory access (DMA) requests to gain control of the UNIBUS.

Input signals from the UNIBUS are received by high-impedance receivers on the DC013 and signals from the DC013 to the UNIBUS are supplied by high-current, open-collector driver outputs. The signals levels between the UNIBUS and the DC013 are compatible. The input and output signals between the device and DC013 are TTL levels.

The DC013 circuits includes bus grant logic, bus busy logic, and slave acknowledge logic. The simplified logic diagram of the DC013 is shown in Figure 1.

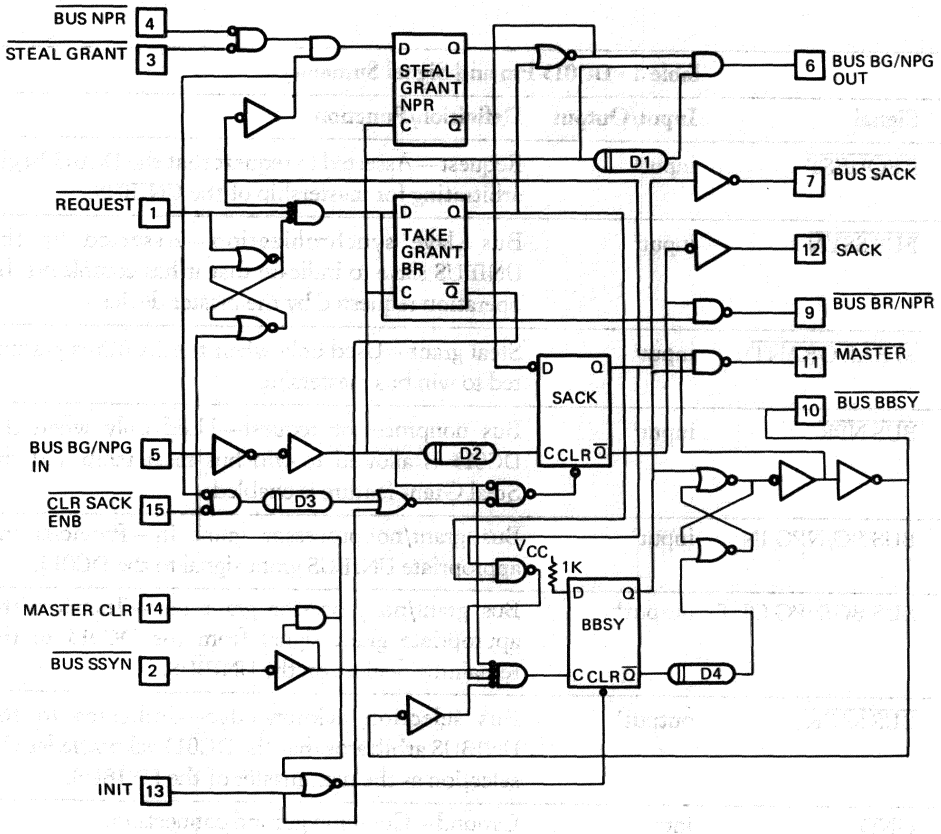

Figure 1 • DC013 Simplified Logic Diagram

• Pin and Signal Definitions

The input and output pins and power and ground connections of the DC013 are shown in Figure 2. Table 1 provides a summary of the signals defined in the following paragraphs.

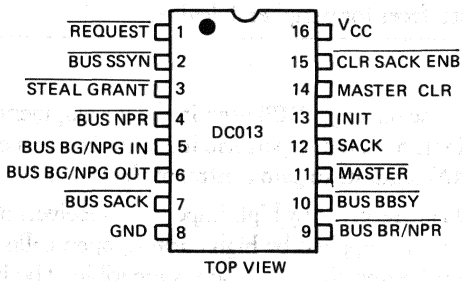

Figure 2 • DC013 Pin Assignments

Table 1 • DC013 Pin and Signal Summary

Pin	Signal	Input/Output	Definition/Function
1	REQUEST	input[1]	Request—Asserted to request that the DC013 begin arbitrating for mastership of the UNIBUS.
2	BUS SSYN	input[2]	Bus slave synchronization—Asserted by the UNIBUS slave to indicate that it has completed the operation requested by the master device.
3	STEAL GRANT	input[2]	Steal grant—Used only when the DC013 is permitted to win bus mastership.
4	BUS NPR	input[2]	Bus nonprocessor request—Used only when the DC013 is allowed to win bus mastership and the Steal Grant feature is enabled.
5	BUS BG/NPG IN	input[2]	Bus grant/nonprocessor grant in—Provides the appropriate UNIBUS grant signal to the DC013.
6	BUS BG/NPG OUT	output[3]	Bus grant/nonprocessor grant out—Transfers the appropriate grant signal from the DC013 to the remaining devices on the UNIBUS.
7	BUS SACK	output[3]	Bus selection acknowledge—Indicates to the UNIBUS arbitrator that the DC013 acknowledges its selection as the next master of the UNIBUS.
8	GND	input	Ground—Common ground connection.

Pin	Signal	Input/Output	Definition/Function
9	$\overline{\text{BUS BR/NPR}}$	output[3]	Bus request/nonprocessor request out—Indicates that the DC013 has been requested by the $\overline{\text{REQUEST}}$ input signal to arbitrate for mastership of the UNIBUS.
10	$\overline{\text{BUS BBSY}}$	input[2]/output[3]	Bus busy—As an input, it informs the DC013 that the current master has completed its use of the UNIBUS. As an output, it allows the DC013 to indicate that it has become the current bus master.
11	$\overline{\text{MASTER}}$	output[1]	Master—Asserted when the DC013 is the current bus master and is asserting the $\overline{\text{BUS BBSY}}$ signal.
12	SACK	output[1]	Selection acknowledge—Asserted when the DC013 is asserting the $\overline{\text{BUS SACK}}$ signal to acknowledge its selection as the next master of the bus.
13	INIT	input[1]	Initialize—Asserted to initialize the DC013.
14	MASTER CLR	input[1]	Master clear—Asserted to allow the $\overline{\text{BUS SSYN}}$ input to clear the DC013.
15	$\overline{\text{CLR SACK ENB}}$	input[1]	Clear selection acknowledge enable—Asserted to allow the UNIBUS arbitration to resume after the DC013 has become bus master.
16	V_{CC}	input	Voltage—Power supply dc voltage.

[1]TTL level
[2]high-impedance UNIBUS input
[3]open-collector UNIBUS output

UNIBUS Signals

$\overline{\text{BUS SSYN}}$—Asserted by the UNIBUS slave to indicate that it has completed the operation reqested by the master device. When the DC013 is used to win interrupt mastership, this input signal indicates that the processor has accepted the interrupt vector and allows the DC013 to release the bus. When the DC013 is used to win DMA mastership, this input may be directly connected to the UNIBUS or to other logic within the master device.

$\overline{\text{STEAL GRANT}}$—When the DC013 is used to win interrupt mastership, this input signal allows it to steal and reply to an interrupt grant intended for another device connected to the UNIBUS. This feature can reduce the overall DMA latency.

$\overline{\text{BUS NPR}}$—When the steal grant feature is enabled and the DC013 requests interrupt mastership, this input informs the DC013 that a DMA device is requesting use of the bus.

$\overline{\text{BUS BG/NPG IN}}$—When the DC013 requests interrupt mastership, this input connects to the appropriate BUS BG7 through BUS BG4 input. When requesting DMA mastership, it connects to the BUS NPG input.

$\overline{\text{BUS BG/NPG OUT}}$—When the DC031 requests interrupt mastership, this output connects to the appropriate BUS BG7 through BUS BG4 output. When the DC013 requests DMA mastership, it connects to BUS NPG output.

BUS SACK—This output indicates to the UNIBUS arbitrator that the DC013 acknowledges its selection as the next master of the UNIBUS.

BUS BR/NPR—This output indicates that the DC013 has been requested by the REQUEST input to arbitrate for mastership of the UNIBUS. If the DC013 is requesting interrupt mastership, this output connects to the appropriate UNIBUS line BUS BR7 through BUS BR4 output. If the DC013 requests DMA mastership, the output connects to the UNIBUS BUS NPR line.

BUS BBSY—After the DC013 has been granted next bus mastership, it must wait for the current master to complete its data transfers. This input informs the DC013 that the current master has completed its use of the UNIBUS and provides an output from the DC013 to indicate that it has become the current master of the UNIBUS.

Device Signals

REQUEST—An input from the device to request that the DC013 begin arbitrating for mastership of the UNIBUS.

MASTER—This output is asserted when the DC013 is asserting the BUS BBSY signal indicating that the DC013 is the current master of the UNIBUS. If the DC013 is requesting interrupt mastership, this output indicates that the interrupt vector from the device should be transferred to the UNIBUS data lines. If the DC013 is requesting DMA mastership, the output is used to trigger tha data transfer logic of the master device.

SACK—This output is asserted when the DC013 is asserting the BUS SACK output to acknowledge its selection as the next bus master.

INIT—This input initializes the logic in the DC013 to end the bus cycle initiated by the DC013.

MASTER CLR—This input allows the BUS SSYN input to clear the DC013 logic. The use of this input is optional when the DC013 is used for DMA transfers.

CLR SACK ENB—This input causes the the DC013 to deassert the BUS SACK output if the DC013 is also asserting the BUS BBSY output. It allows UNIBUS arbitration to resume when the DC013 becomes bus master. When the DC013 is requesting DMA mastership, this output may be used to delay UNIBUS arbitration during multiple data cycles. During the last data cycle, the the master logic should assert the CLR SACK ENB input to the DC031 to allow the arbitration to be resumed.

Power and Ground Connections

Supply voltage (V_{cc}): Connects to the 5-Vdc power supply

Ground (GND): Common signal and voltage ground

• Functional Operation

The following descriptions assume that the reader has a knowledge of the operation of the UNIBUS. Refer to the *PDP-11 UNIBUS Processor Handbook PDP-11/84, PDP-11/44, and PDP-11/24* (Digital document no. EB 26077-41) for a more detailed description of the UNIBUS operation.

Typical UNIBUS interface implementation of the DC013 for interrupt and DMA data transfers is shown in Figure 3. Request and grant signals that are not used are wired through the interface and can be used by subsequent devices.

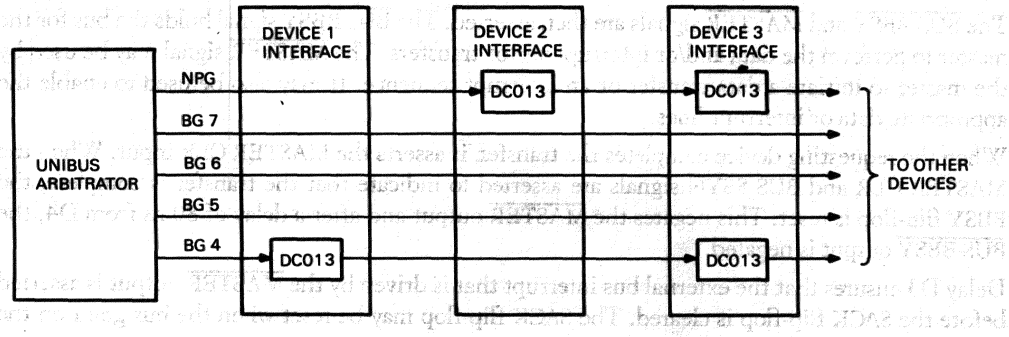

Figure 3 • DC013 Typical DMA and Interrupt Request Configuration

The signals designations, shown in the DC013 control logic Figure 1, that are preceded by a "BUS" designation connect to the UNIBUS lines. The DC013 contains the control logic required for a device to become bus master. A bus master can request and gain control of the UNIBUS to transfer interrupt vectors or data.

The two types of requests that can be initiated are the interrupt bus request (BR) and direct memory access (DMA) nonprocessor request (NPR). A device that requires use of the bus to transfer data or vectors through an interrupt initiates a BR to the arbitrator in a CPU or controller. A BR results in a processor interrupt and the request, grant, and data transfer constitute an interrupt transaction. Only one interrupt transaction may be executed under a single grant.

The NPR is assigned the highest priority and solicits the use of the data section of the bus to transfer data between a device and memory without active participation of the processor. A device that requests the use of the bus sends an NPR to the arbitrator in the CPU when the device is ready to transfer data.

The assertion of the $\overline{\text{REQUEST}}$ input initiates a priority transfer sequence and is applied to the D input of the Take Grant flip-flop. This flip-flop ensures that only one priority transfer sequence is initiated for each $\overline{\text{REQUEST}}$ input. If the requesting device is not presently bus master, the BBSY flip-flop is not set. For each request the $\overline{\text{REQUEST}}$ signal must be negated and again asserted before another cycle can begin.

The state of the $\overline{\text{BUS BBSY}}$ signal determines whether the received bus grant signal (BUS BG/NPG IN) is transferred to the next device or is accepted by the requesting device. If $\overline{\text{BUS BBSY}}$ is not asserted, the logic accepts the grant. If $\overline{\text{BUS BUSY}}$ is asserted, the grant is passed to another device of the same priority level.

The BUS BG/NPG IN signal clocks the Take Grant and Steal Grant flip-flops. With the $\overline{\text{REQUEST}}$ input asserted, the Take Grant flip-flop is set or if another device is asserting the $\overline{\text{BUS NPR}}$ input and the $\overline{\text{STEAL GRANT}}$ input is asserted, the Steal Grant flip-flop is set. Either flip-flop when set disables the bus grant driver and negates the BUS BG/NPG OUT signal. When the grant is accepted, the SACK flip-flop is set after the 75 ns delay from D2. The delay D2 ensures that the Take Grant and Steal Grant flip-flops have time to respond to the BUS BG/NPG IN signal before the SACK flip-flop is clocked. When the Sack flip-flop is set, the $\overline{\text{BUS SACK}}$ output is asserted and the arbitrator is allowed to negate the grant after a minimum of 75 ns and the bus request signal $\overline{\text{BUS BR/NPR}}$ is negated. The BBSY flip-flop is set when the clock input conditions have been satisfied. This occurs when the Take Grant and Sack flip-flops are set and the BUS BG/NPG IN, $\overline{\text{BUS SYNC}}$, and $\overline{\text{BUS BBSY}}$ signals are negated.

The BUS BBSY and MASTER signals are then asserted. The BUS BBSY signal holds the bus for the master to perform the data and/or interrupt vector transfers. The MASTER signal may be used by the master to initiate a data transfer or an interrupt sequence. It may also be used to enable the appropriate data or interrupt lines.

When the requesting device completes the transfer, it asserts the MASTER CLR input. When the MASTER CLR and BUS SSYN signals are asserted to indicate that the transfer is complete, the BBSY flip-flop is reset. This negates the MASTER output and after a delay of 80 ns from D4, the BUS BBSY output is negated.

Delay D3 ensures that the external bus interrupt that is driven by the MASTER output is asserted before the SACK flip-flop is cleared. The SACK flip-flop may be reset when the bus grant on the BUS BG/NPG IN input is negated.

Asserting the INIT input clears the BBSY flip-flop if the bus grant signal BUS BG/NPG input is negated.

A device not requesting the bus may assert the STEAL GRANT input to improve NPR latency. It then receives an BUS NPR input followed by a bus grant signal BUS NPG IN. It blocks the bus grant intended for a another device and asserts the BUS SACK signal that causes the arbitrator to negate the bus grant signal and stop the arbitration. The negation of the BUS BG/NPG IN signal resets the SACK flip-flop.

A device closer to the arbitrator may assert a BUS NPR signal before a grant is issued to a device that previously made a bus request. The arbitrator first honors the NPR and issues an NPG. When the NPR device has completed its transaction, the arbitrator issues a bus grant to the original device.

Interfacing Techniques

The DC013 control logic is used to develop device interfaces to generate bus interrupt and nonprocessor request. The following paragraphs describe the use of the DC013 and standard circuits for typical interface applications.

Bus Request Logic

A typical BR UNIBUS interface using the DC013 and standard ICs for the bus drivers and receivers is shown in Figure 4. This circuit generates one interrupt vector address and transfers the address and data to the UNIBUS. The 8641 ICs can be replaced with two DC021 Octal Bus Transceivers. The interrupt vector from the 74157 ICs is multiplexed with the data lines from the device. The address is selected by inserting and removing jumper leads (V2 through V8). Multiplexing the inputs before the bus drivers reduces the total UNIBUS loading of the device.

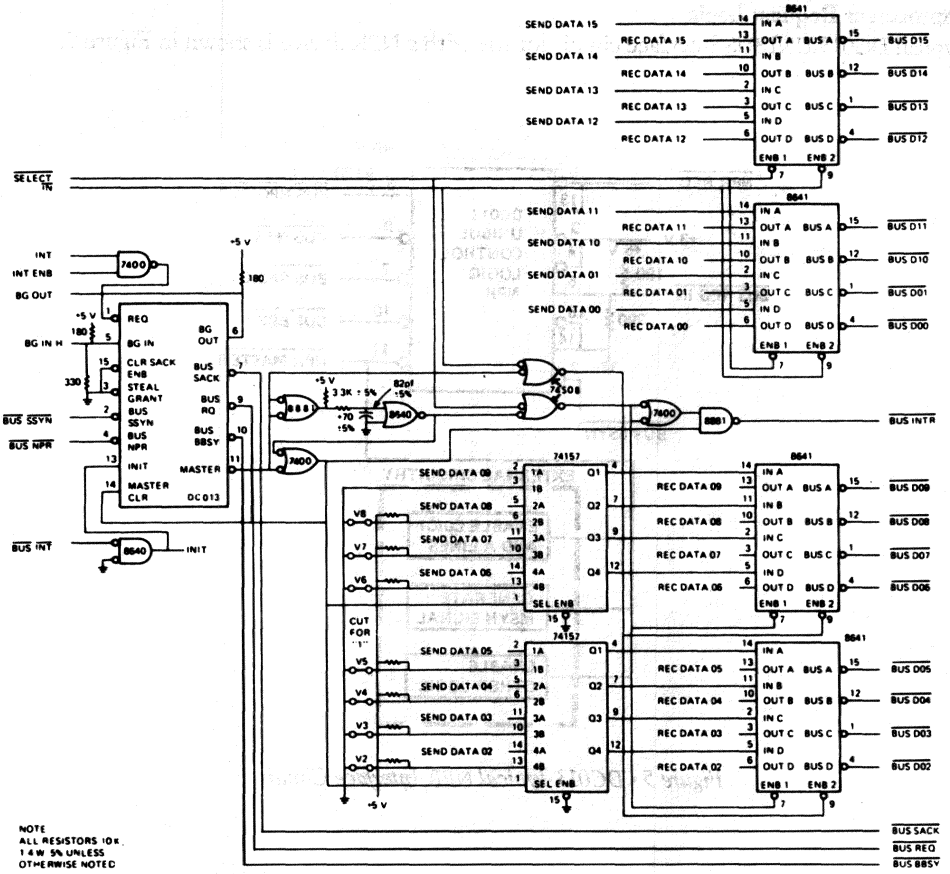

Figure 4 • DC013 Typical BR Interface Circuit

A bus request is initiated by a device when an interrupt is required. The INT ENB signal is normally produced by a bit in the control and status register of the device. When the INT ENB and the INT inputs from the device are asserted, the $\overline{\text{REQUEST}}$ input to the DC013 is asserted to initiate a priority transfer sequence on the UNIBUS. When the device receives the grant, the $\overline{\text{MASTER}}$ output is asserted and begins the interrupt sequence.

The master device negates both the $\overline{\text{SELECT}}$ and $\overline{\text{IN}}$ inputs to disable the UNIBUS transceivers for the D<01:00> and D<15:10> lines.

When the $\overline{\text{SELECT}}$ input to the multiplexer is negated, the A inputs are transferred to the bus. When the SELECT input is asserted, the B inputs are transferred to the bus.

The assertion of the $\overline{\text{MASTER}}$ output enables the SEL inputs to the multiplexers, enables the outputs of the bus transceivers lines BUS D<09:02> and, after a delay, it enables the remaining input to the gate that generates the $\overline{\text{BUS INTR}}$ output. The interrupt vector is therefore available before the interrupt is requested that complies with the bus specifications. When the processor receives the $\overline{\text{BUS INTR}}$ signal, it reads the vector information on the bus and asserts the $\overline{\text{BUS BBSY}}$ signal. The device receives this signal, deasserts the $\overline{\text{MASTER}}$ output to terminate the vector, and deasserts the $\overline{\text{BUS INTR}}$ output. After a delay of 80 ns, it deasserts the $\overline{\text{BUS BBSY}}$ output.

Nonprocessor Request Logic

A typical DC013 UNIBUS interface circuit for use with a NPR device is shown in Figure 5.

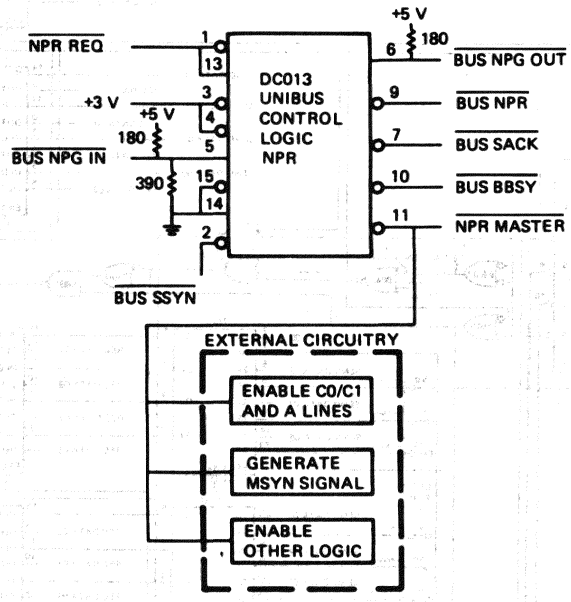

Figure 5 • DC013 Typical NPR Interface Circuit

When an NPR transfer is required, the requesting device asserts the NPR REQ input. The arbitrator recognizes this request and issues a nonprocessor grant by asserting the BUS NPG IN input. The requesting device blocks the grant from being transferred to the next device interface and acknowledges the grant by asserting the BUS SACK output. With this signal asserted, the arbitrator negates the grant and stops the arbitration process. With BUS SACK asserted, the arbitrator negates the grant and stops arbitrating. When the requesting device receives the negation of the BUS BBSY, BUS SSYN, and BUS NPG signals, it asserts the BUS BBSY output, becomes bus master, and initiates the data transfer.

The NPR MASTER output, asserted when the BUS BBSY signal was asserted, is used to drive the external circuits. When the data transfer is complete, the device negates the NPR REQ input to relinquish the bus mastership. The NPR REQ input connects to the INIT input (13). Once a request is initiated, the NPR REQ input must remain asserted until the data transfer is complete to prevent the premature termination of bus mastership.

The Steal Grant flip-flop is disabled by connecting the STEAL GRANT (3) and BUS NPR (4) inputs to 3 V. The BUS NPG input is held asserted by the resistor network. The CLR SACK ENB (15) is asserted and the MASTER CLR input is negated by the ground connection that allows only one bus cycle for each request. For more than one data cycle, the CLR SACK ENB input can be held negated until the beginning of the last bus cycle.

An interrupt request cannot be performed by a device that has become bus master through an NPR. In most NPR applications, an interrupt request usually follows the completion of a set of NPR transfers. This interrupt may be used to notify the processor that the NPR transfers are complete or that an error has occurred during the data transfer.

Bus Loading Configuration

A typical device interface that uses a DC013 for NPR control and a DC013 for BR transfers is shown in Figure 6. The UNIBUS loading for the BUS SACKand BUS BBSY outputs can be reduced by using the wired-OR configurations from the DC013 outputs as shown.

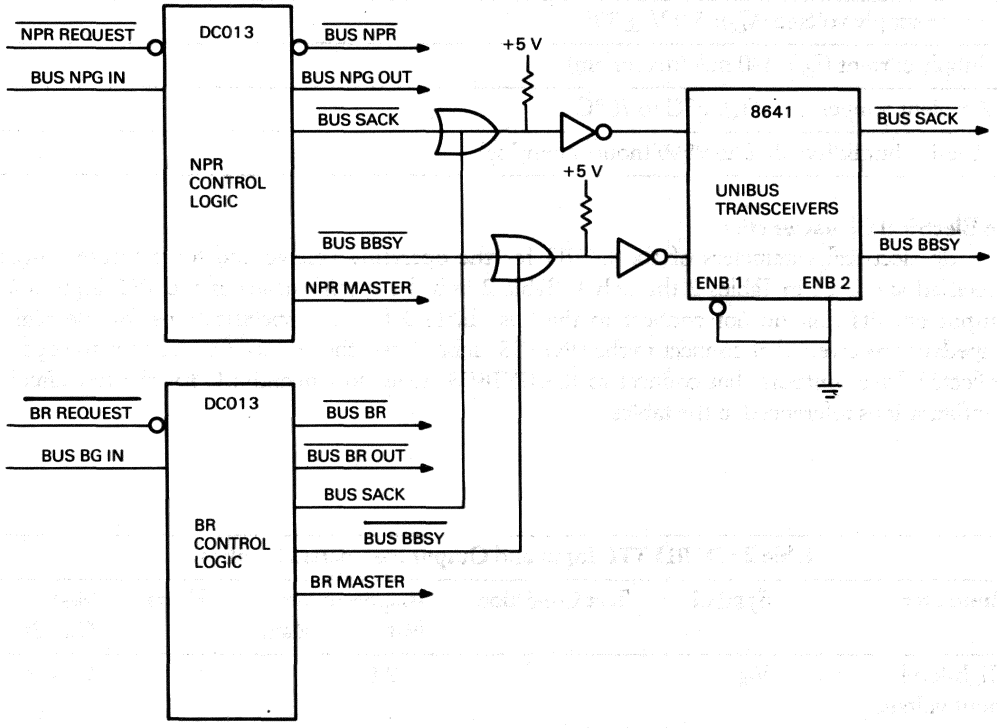

Figure 6 • DC013 BR and NPR Wiring Configuration

• Specifications

The mechanical, electrical, and environmental characteristics and specifications for the DC013 are described in the following paragraphs. The test conditions for the electrical values are as follows unless specified otherwise.

- Ambient temperature (T_A): 0°C to 70°C
- Supply voltage (V_{CC}): 5.0 V ±5%

Absolute Maximum Ratings

Stresses greater than the absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum ratings for extended periods may adversely affect the reliability of the device.

- Supply voltage (V_{CC}): 7.0 V
- Input voltage (V_I): 5.5 V
- Ambient temperature (T_A): 0°C to 70°C
- Storage temperature (T_S): −65°C to 125°C

Recommended Operating Conditions

- Power supply voltage (V_{CC}): 5.0 V ±5%
- Supply current (I_{CC}): 140 mA (maximum)
- Ambient temperature (T_A): 0°C to 70°C
- Relative humidity: 10% to 95% (noncondensing)

dc Electrical Characteristics

The dc electrical parameters of the DC013 for the operating voltage and temperature ranges specified are listed in Tables 2 through 4. Table 2 lists the specifications of the TTL input and output circuits that do not connect to the bus. Table 3 lists the specifications for the high-impedance receivers that connect to the UNIBUS. Table 4 lists the dc specifications for the open-collector driver outputs that connect to the UNIBUS. Refer to Appendix C for the test circuit configurations referenced in the tables.

Table 2 • DC013 TTL Input and Output Parameters (nonbus)

Parameter	Symbol	Test Condition	Requirements Min.	Requirements Max.	Units	Test Circuit
High-level input voltage	V_{IH}		2.0	—	V	C1,C2
Low-level input voltage	V_{IL}		—	0.8	V	C1,C2
Input clamp voltage	V_I	V_{CC}=open I_I=−18 mA	—	−1.2	V	C3
High-level output voltage	V_{OH}	V_{CC}=4.7 V I_O=−1.0 mA	2.7	—	V	C1
Low-level output voltage	V_{OL}	V_{CC}=4.75 V				C2
pin 11		I_O=20 mA[1]	—	0.5	V	
pin 12		I_O=2 mA	—	0.5	V	

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
Input current at maximum input voltage	I_I	$V_{CC}=5.25$ V $V_I=5.5$ V	—	1.0	mA	C3
High-level input current	I_{IH}	$V_{CC}=5.25$ V $V_I=2.7$ V				C4
pins 13,15			—	50	µA	
pins 1,14			—	100	µA	
Low-level input current	I_{IL}	$V_{CC}=5.25$ V $V_I=0.5$ V				C5
pin 15			—	-0.55	mA	
pin 1,13,14			—	-1.1	mA	
Short-circuit output current	I_{OS}	$V_{CC}=5.25$ V[2]				C6
pin 11			-40	-100	mA	
pin 12			-5.0	-45	mA	
Supply current	I_{CC}	$V_{CC}=5.25$ V	—	140	mA	C7

[1]Requires a load current of 70 mA at pin 10.
[2]Not more than one output shall be short circuited at a time and the duration of the short shall not exceed 1 second.

Table 3 • DC013 High-impedance Bus Receiver Parameters

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
High-level input voltage	V_{IH}	$V_{CC}=4.75$ V	1.53	—	V	C1,C2
		$V_{CC}=5.25$ V	1.70	—	V	
Low-level input voltage	V_{IL}	$V_{CC}=4.75$ V	—	1.30	V	C1,C2
		$V_{CC}=5.25$ V	—	1.47	V	
Input clamp voltage	V_I	$V_{CC}=4.75$ V $I_I=-18$ mA	—	-1.2	V	C3
High-level input current*	I_{IH}	$V_{CC}=0$ V $V_I=3.8$ V	—	40	µA	C4
		$V_{CC}=5.25$ V	—	40	µA	
pin 10		$V_{CC}=0$ V	—	40	µA	
pin 10		$V_{CC}=5.25$ V	—	65	µA	

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
Low-level input current*	I_{IL}	$V_{CC}=0$ V $V_I=0$ $V_{CC}=5.25$ V $V_I=0$	— —	-10 -10	μA μA	C5
pin 10		$V_{CC}=0$ V $V_I=0.5$ V	—	-10	μA	
pin 10		$V_{CC}=5.25$ V $V_I=0.5$ V	—	-10	μA	

*All pins except pin 10.

Table 4 • DC013 Open-collector Bus Driver Parameters

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
Output reverse current*	I_{OH}	$V_{CC}=4.75$ V $V_{OH}=3.5$ V	—	25	μA	C1
pin 10			—	65	μA	
Low-level output voltage	V_{OL}	$V_{CC}=4.75$ V $I_{sink}=70$ mA $I_{sink}=16$ mA	— —	0.8 0.5	V V	C2

*All pins except pin 10.

ac Electrical Characteristics

The input/output signal timing for the UNIBUS request logic is shown in Figure 7. The transient specifications for the signals are listed in Table 5. Refer to Figure 8 for the load circuits used in measuring the TTL outputs and open-collector outputs. Refer to Appendix D for the voltage waveforms used in measuring the propagation delays.

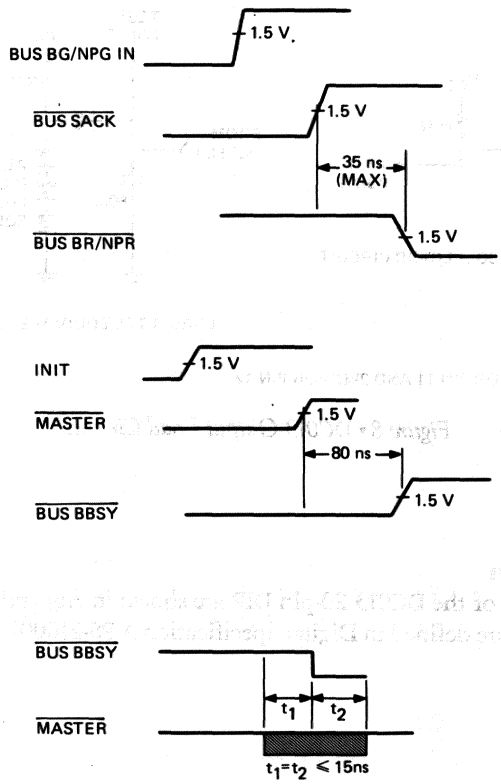

Figure 7 • DC013 Signal Timing Sequence

Table 5 • DC013 ac Signal Transient Specifications

Signal	Input Voltage	Parameters (ns) Rise Time	Fall Time
REQUEST	0 to 3	≥ 15	≥ 6
CLR SACK ENB	0 to 3	≥ 15	≥ 6
MASTER CLR	0 to 3	≥ 15	≥ 6
INIT	0 to 3	≥ 15	≥ 6
BUS NPR	1 to 2	≥ 10	≥ 10
STEAL GRANT	1 to 2	≥ 10	≥ 10
BUS BG/NPG IN	1 to 2	≥ 10	≥ 10
BUS SSYN	1 to 2	≥ 10	≥ 10
BUS BBSY	1 to 2	≥ 10	≥ 10

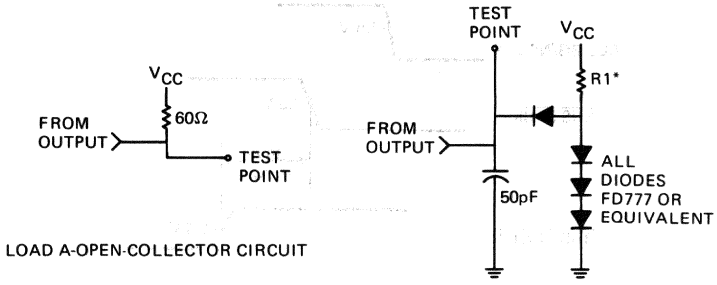

Figure 8 • DC013 Output Load Circuits

Mechanical Configuration

The physical dimensions of the DC013 20-pin DIP are shown in Appendix E. The materials and construction of the DIP are defined in Digital Specification A-PS-210002-GS.